REMARKS

The undersigned wishes to thank the Examiner, Mr. Mujtaba Chaudry, for the courtesies shown during an interview in the case on September 22, 2003.

The substantial difference between the Applicant's invention and the reference to Schwartz was discussed during the interview. The Examiner admitted that proposed claim amendments to include "initialization storage means" into independent claims 1 and 8 requires additional search, but make the claimed invention distinguishable over the reference to Schwartz. Additionally, the Examiner pointed out on ambiguity of claim language which was corrected by this amendment.

Minor corrections for the specification are entered by this amendment.

Claims 1, 3-8, 10-17 are currently pending in the application. By this amendment, claims 1, 3, 8, 12, and 17 are amended and claims 2 and 9 are canceled. Specifically, the limitation of claims 2 and 9 are incorporated into claims 1 and 8 accordingly. Support for the amendments is provided in at least Figure 4 and at pages 13-14 of the present specification. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Claims 1, 8, 12 and 17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed based on the following discussion.

The Examiner pointed out several issues, which form a basis for indefiniteness of the claims. First, the Examiner states that "claim 1 recites in part, "... a built-in self-test arrangement..." which is not clear". Further the Examiner suggests "to link the BIST arrangement with the actual integrated circuit and explicitly state that in the claim language". Applicant respectfully disagrees with this proposal and refers to the Examiner to MPEP 2106, which mandates, "...the **definiteness of the language must be analyzed, not in a vacuum, but always in light of the teachings of the disclosure** as it would be interpreted by one of ordinary skill in the art." It should be respectfully noted that the present specification recites and explains in detail what the Applicant implies as a built-in self-test arrangement, see page 4, lines 9-22, and

page 5, lines 20-25. According to the disclosure, the term of "built-in self-test arrangement"means a self-test circuit on the chip.

The second issue noted in the office action is related to the, as the Examiner states, "excessive usage of the term means". The Examiner does not cite any authority concerning statutory limitation in this regard. However, MPEP §2106 clearly approves a usage of means plus function limitation and defines it as "the corresponding structure or material set forth in the written description and equivalents". Furthermore, "Such means may be defined as: .... -a logic circuit or other component of a programmed computer that performs a series of specifically identified operations dictated by a computer program;...".

Next, the Office Action states that it is not clear for the Examiner if the "means for discriminating a source of test command" is included within the "means for storing test instruction" or in the integrated circuit. Figure 1 of the disclosure shows that the instruction storage 30 structurally connected to programmable memory BIST controller 10, which performs discriminating function.

Furthermore, the Examiner objected of usage of terms "test command" and "test instruction". According to the original disclosure "test instruction" relates to the test algorithm and represents commands within any particular test. (See specification page 6, lines 22-25) The term "test command" relates to a command for choosing a test among others, in the present case it could be board, system or manufacturing type of test. Claim 1 specifies, "means for storing test instruction including means for discriminating a source of a test command for performing manufacturing level and board level testing and receiving test instructions provided from an external tester,...". This operation is described in greater detail on page 15, lines 9-30 of the present specification.

The Examiner also objected the part of the claims which states, "performing manufacturing level and board level testing". The Examiner points out that this wording specifies synchronous performance of both test at the same time. Applicant is not quite agree for the reason that all claims are apparatus claims, not method. However, the amendment of claims language in order to replace "and" with "or", as the Examiner advised, has been done. Specifically, Claims 1, 8 and 17 have been amended.

Claims 1-17 were rejected under 35 U.S.C. §102(e) as being unpatentable over Schwartz. This rejections respectfully traversed based on the following discussion.

The present invention uses not only default test instructions, but in addition, inputs test instructions which are stored within BIST-arrangement. It should be noted that manufacturing and board level tests require initialization which is provided by Initialization Storage Module 210 of Figure 4 with a default set of test instructions. This feature allows Applicant's test to be more flexible compared to Schwartz and does not require an external tester for performing. In contrast, the reference to Schwarz is confined to embedded device tests which require no initialization and needs an external tester.

In order to emphasize this feature claim 1 has been amended. Specifically the limitations of claim 2 was incorporated into claim 1, and claim 2 canceled. Claim 1 as amended now recites,

> "...means for storing test instructions and discriminating between performing manufacturing level or board level testing and receiving test instructions provided from an external tester,
>
> means for generating default test instructions **for performing manufacturing level or board level testing**, and
>
> means for supplying said default test instructions **for performing manufacturing level or board level testing** to said means for storing test instructions,
>
> **wherein said means for generating default test instructions includes an initialization storage means**."

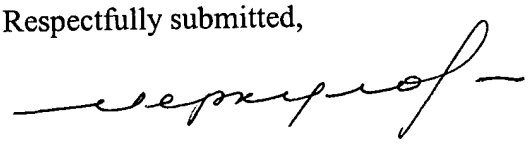
MPEP 2131 states that "To anticipate a claim, the reference must teach every element in the claim". Furthemore, the MPEP, citing Richardson v. Suzuki Motor CO., 9 USPQ2d 1051, 1053 (Fed. Cir. 1987), states, "the identical invention must be shown in as complete details as is contained in the ...claim."

Here, the means for generating default test instructions which includes an initialization storage means is not shown by the reference to Schwartz. It is therefore respectfully submitted

that the rejection to the claims is improper under §102 as Schwartz cannot anticipate the rejected claims since it does not "teach an identical invention". Further, since the initialization limitation is not taught or suggested by reference, Schwartz cannot be used to support a *prima facie* obviousness under §103. Based on the above discussion with reference to the MPEP guidelines, it is respectfully requested that the rejection based on 35 U.S.C. §102 be withdrawn and claims be allowed.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims as amended are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458 (IBM Fishkill).

Respectfully submitted,



Olga V. Merkoulova
Registration No. 48,757

Whitham, Curtis & Christofferson, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557
Customer No.: 30743